IKONAS GRAPHICS SYSTEMS INC
403 GLENWOOD AVE — RALEIGH NC 27603 — 919/833-5401

THE IKONAS PROCESSOR AND SEQUENCER

The IKONAS processor is implemented using the Advanced Micro Devices Am2903 bipolar bit slice processor and the Am2911 bit slice microprogram sequencer. A familiarity with these two components will ease understanding of the IKONAS processor, BMP 32, and the microprogram sequencer, MPS 16. A bibliography of introductory literature about bit slice processors and microprogramming is attached. The Applications Notes and Microprogramming Handbook available from AMD are particularly helpful.

The IKONAS processor operates on 32 bit wide words. The processor is controlled by a sequence of microcode words (microprogram) that are 64 bits wide and are stored in static RAM microcode memory. Microprograms are downloaded from the host processor before execution. Programs may be stored in ROM memory. Each microinstruction executes in 200 nsec. Next address selection (program flow control) uses 32 bits of each microcode word. The remianing 32 bits of microcode control ALU function and operand selection. The IKONAS processor and sequencer operation will be discussed in terms of the 64 bit microcode word. Important features of the processor and sequencer will be emphasized as they effect the microcode.

MICROPROGRAM SEQUENCER CONTROL

Figure 1 is a block diagram of the MPS 16. Note the DATA FIELD REGISTER and the path from it to the LOOP COUNTER and the BMP 32. The CONTROL PROM, CONDITION CODE MULTIPLEXER, and the path from the MICROCODE LATCH to the IKONAS FUNCTION BUS are other important features. The sequencer, through the Am2911 and its related circuitry, uses the information in the microcode word and from the condition code lines to generate the 16 bit next address in the microprogram memory. Maximum size of the microprogram memory is 64K words, each 64 bits wide.

The lower 32 bits of a microcode word are inputs to the sequencer for next address selection. The bits are divided into the following fields:

DATA FIELD
OP CODE
CONDITION CODE SELECT
CONDITION CODE PARITY SELECT
LOAD CONTROL
IKONAS BUS FUNCTION CODE

DATA FIELD: Depending on the OP CODE and LOAD CONTROL bits, the 16 bit data field may be used as a pipeline address (D input to the 2911), ALU immediate data, or loop count.

OP CODE: The OP CODE determines what type of program control instruction is to be executed--that is, it addresses the CONTROL PROM which determines the next microcode address depending on the result of the condition code test. The Am2911 sequencer can output next microprogram address from one of four inputs: the data field (D), the 4 word on chip stack for subroutines and loops (F), the microprogram counter (PC), or an on chip latch which is loaded with the D data from the previous instruction (R). Features of the 2911 allow loops and subroutines to be executed with no overhead cycles. The CONTROL PROM has essentially the same instruction set as the Am29811A. Since the instruction set is in firmware, it can be changed or expanded.

CONDITION CODE SELECT: Condition codes are used to control conditional execution of the OP CODES. The condition code select bits choose 1 of 16 conditions to be tested. Presently implemented conditions are: counter=Ø, Host Request Line High, IKONAS BUS busy, IKONAS BUS or IMAGE MEMORY busy, Video Blanked, ALU overflow, ALU negative, ALU zero, and ALU carry out. Other specific condition codes can be easily added.

CONDITION CODE PARITY SELECT: This bit determines whether the conditional operation takes place on condition TRUE or condition FALSE.

LOAD CONTROL: Load Control determines whether the data field will be latched into the loop counter on the MPS 16 or into the immediate data register on the BMP 32.

IKONAS BUS FUNCTION CODE: This field controls read and write operations in Static RAM (32 bit parallel format), Dynamic RAM (512x512 or 1Ø24x1Ø24 format), or other special purpose devices (matrix multiplier, disk controller, etc.).

PROCESSOR CONTROL

In the processor block diagram, Figure 2, the important features are the 16 GENERAL PURPOSE REGISTERS, SELECTORS, and SHIFTERS within the 29Ø3, the R BUS SELECTOR and its sources, the Y BUS, the MDR, MAR, and IMMEDIATE DATA REGISTER and their paths to the IKONAS DATA and ADDRESS busses. The 16 general purpose registers are dual ported RAM with two independent address ports (A and B) and two independent output latches. Data may be written into the registers only using the B address port.

The 32 bits of microcode which are input to the processor are divided into the following fields:

R OPERAND SELECT
S OPERAND SELECT
ALU INSTRUCTION
ALU CARRY CONTROL
ALU SHIFT CONTROL
Y BUS SOURCE/DESTINATION
DR BUS DATA SOURCE
IKONAS BUS ADDRESS SOURCE
IKONAS BUS ENABLE

R OPERAND SELECT: This field selects one of the general purpose registers (Ø-15) or the R bus as the R operand. The field contains bits for A address and R bus select control. The R BUS data may be selected from the data registers (DR), lower 16 bits of DR, Memory Address Register (MAR), lower 16 bits of MAR, or the B register data in several forms: right rotated 8 or 16 bits, right shifted 8 or 16 bits.

S OPERAND SELECT: This field selects one of the general purpose registers (Ø-15) or the Q register as S operand. The B address bits within this field are also used to specify one of the general purpose registers as Y BUS output destination.

ALU FUNCTION: The IKONAS processor, using 8 Am29Ø3's, can perform 7 arithmetic and 9 logical operations on two 32 bit operands. In addition the Am29Ø3 can perform 9 special functions--principally multiplication, division, and normalization. See the Am29Ø3 data sheets for details of the available operations. This field also contains bits selecting shift type (logical or arithmetic) and direction (left or right) for the ALU shifter and Q shifter. Q register and B register write control are also contained in this field.

ALU CARRY CONTROL: Carry control circuitry is designed to allow operands to be treated as two 16 bit words or as one 32 bit word. In double 16 bit format $C_{in}Ø$ and $C_{in}16$ may be set to either 1's or Ø's. In 32 bit format, $C_{in}Ø$ may be set to Ø, 1, $C_{out}31$, or $C_{out}31$ inverted.

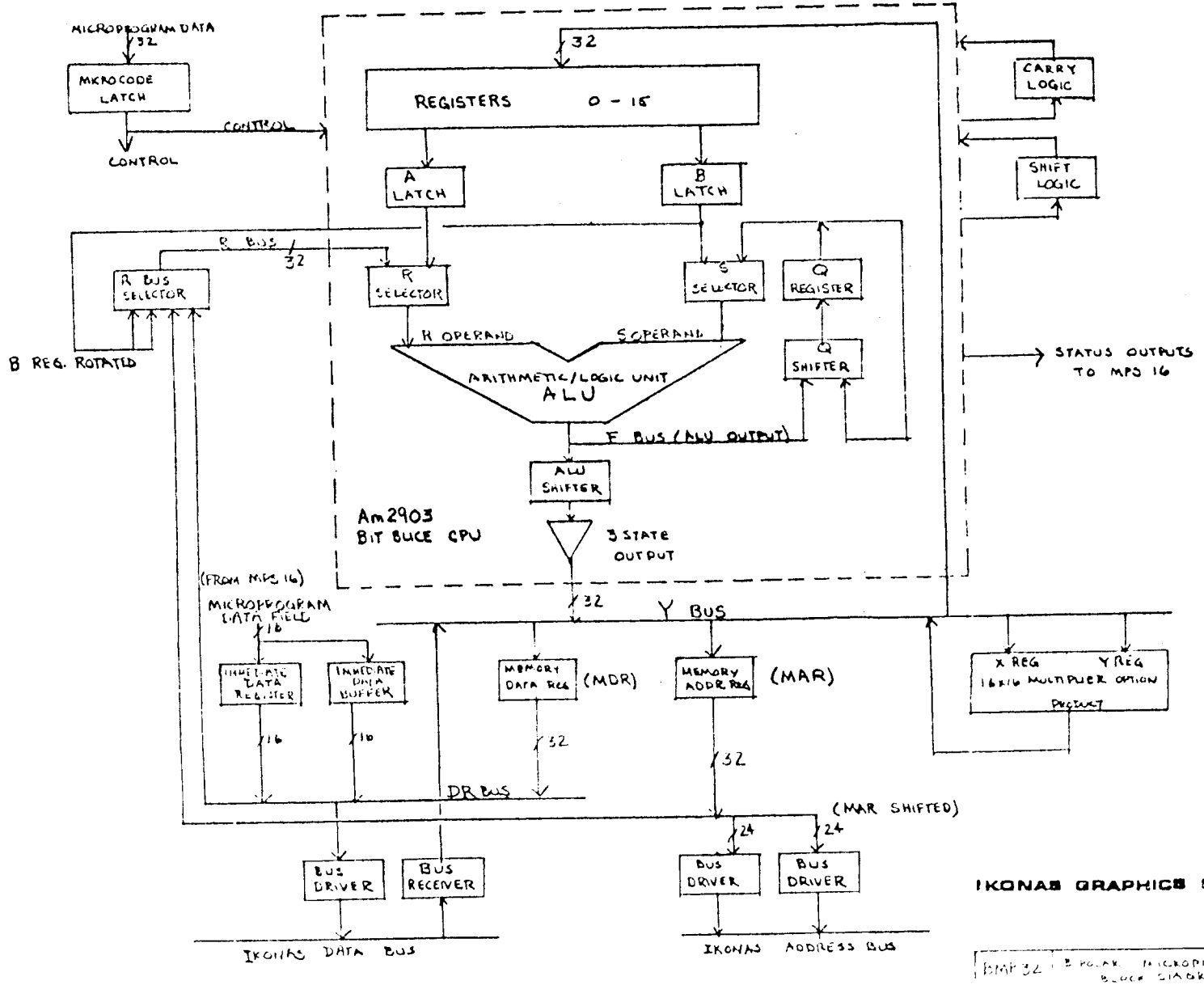
ALU SHIFT CONTROL: The ALU and Q shifters may be used to shift or rotate data. This field controls whether a shift or rotate is performed and whether the operations are long (64 bits using ALU and Q shifters as a unit) or short (using ALU and Q shifters as independent 32 bit units). The shift input (Ø or 1) is determined by this field. (Recall that direction and type of shift are controlled by the ALU FUNCTION field.)

Y BUS SOURCE/DESTINATION: The Y BUS is a communication path among the Am29Ø3 ALU general purpose registers, several special purpose registers, and an optional hardware multiplier. Possible sources of data on the Y BUS are the ALU output, the IKONAS BUS, and the multiplier output. Destinations possible are the general purpose registers (using the B address), the MDR, the MAR, and the multiplier inputs X and Y. When set up in the appropriate fields, the general purpose registers may be a second destination for data being written to the MDR, MAR, or multiplier inputs.

DR BUS DATA SOURCE: This field determines the data source for the DR bus. Data may come from the MDR or from the microcode data field for immediate operands.

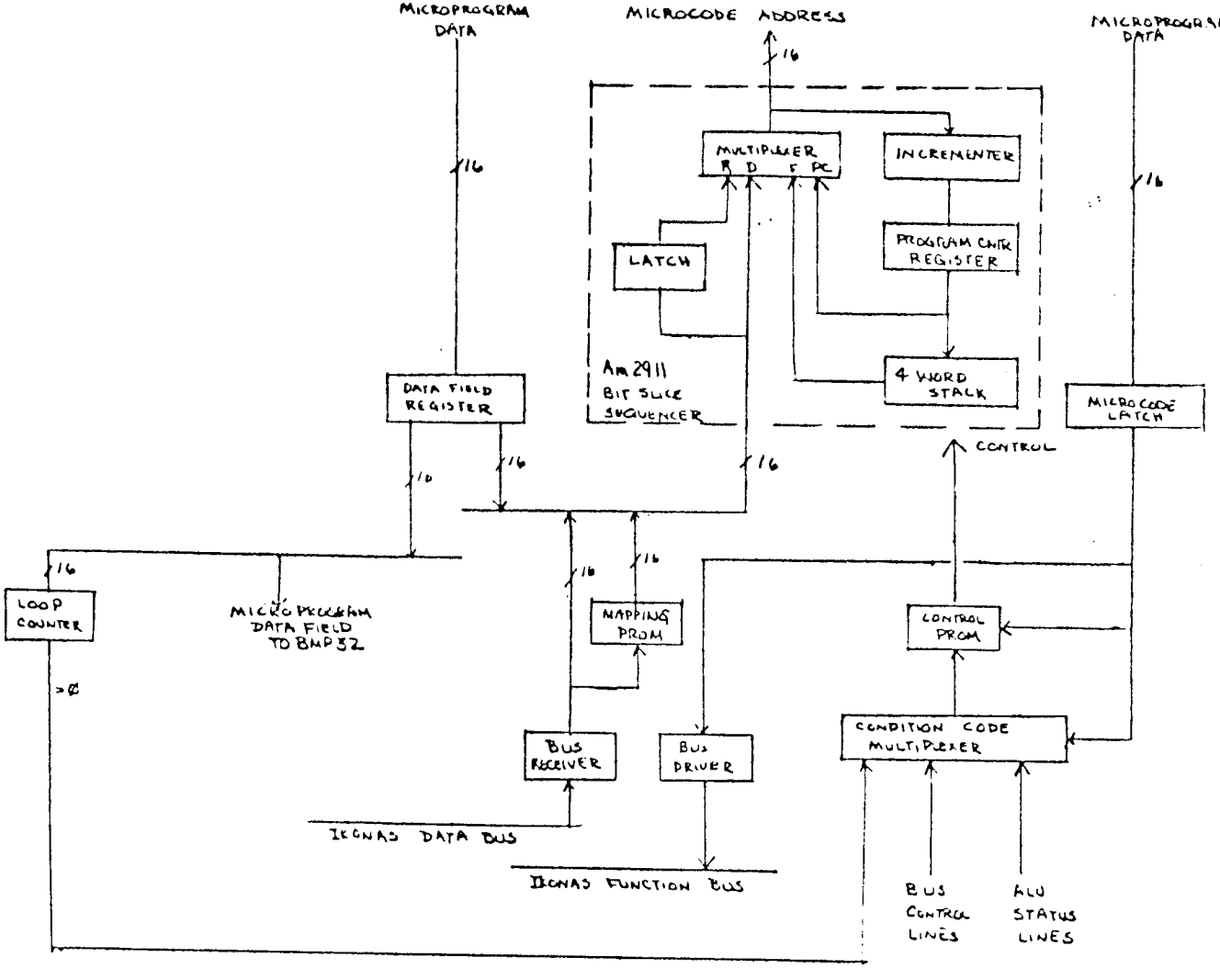
IKONAS BUS ADDRESS SOURCE: For IKONAS BUS read and write cycles address data may come from the MAR directly or from the MAR shifted such that frame buffer X and Y addresses stored in upper and lower half words are packed into a single 24 bit address.

IKONAS BUS ENABLE: When set =1, this bit causes a Read or Write cycle on the IKONAS BUS.



IKONAS GRAPHICS SYSTEMS, INC.

IMAP 32	32 BIT BIPOLAR MICROPROCESSOR BLOCK DIAGRAM	1 of 1 8/79



IKONAS GRAPHICS SYSTEMS, INC.

MPS16	MICRO PROGRAM SEQUENCER BLOCK DIAGRAM	1 of 1 8/79

IKONAS GRAPHICS SYSTEMS INC
403 GLENWOOD AVE — RALEIGH NC 27603 — 919/833-5401

A BRIEF BIBLIOGRAPHY ON MICROPROGRAMMING AND BIT-SLICE PROCESSORS

I. Publications of Advanced Micro Devices, Inc.
901 Thompson Place
Sunnyvale, CA 94086
(available through Hamilton Avnet)

The Am2900 Family Data Book
Note: 2903, 2911 are major building blocks of the IKONAS processor IKASM^{tm}, the IKONAS cross assembler for microcode,is similar to ADASM

Microprogramming Handbook, John R. Mick and Jim Brick
Publication Number: AM-PUB029
Essentially a refinement of articles appearing in EDN, vol.23 no.2,3,4; January 20, February 5, February 20, 1978.

Microprogram Design with the Am2900 Family
Publication Number: AM-PUB069

Build a Microcomputer--Chapter II Microprogrammed Design
Publication Number: AM-PUB073-2

Applications literature for the Am2903

II. Articles

"A primer on bit-slice processors", John Nemec, Electronic Design, February 1, 1977.

"Use 4-bit slices to design powerful microprogrammed processors", Jim Clymer, Electronic Design, May 10, 1977.

"Microprogramming: Making your mini move faster", John Trudeau, Digital Design, January, 1977.

"Bipolar μP's: Introduction to architecture and applications", John Nemec and Stephen Y. Lau, EDN, September 20, October 4, 1977.

"Microgrogramming: A General Design Tool", Robert Jaeger, Computer Design, August 1974.

III. Book

Microprogrammable Computer Architectures, Alan B. Salibury, Elsevier Computer Science Library, American Elsevier Publishing Co., Inc. New York, 1976.